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Essentials of Electronic Testing for Digital, Memory and
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Bushnell, Michael L., and Vishwani D. Agrawal. Essentials of Electronic Testing for Digital, Memory, and Mixed-signal VLSI Circuits. New York, NY: Springer, 2000. Syllabus This course examines the theory and practice of fault analysis, test generation, and design for testability for digital circuits and systems.

~~EECS 579 | Electrical & Computer Engineering at Michigan~~

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Signal Boundary-Scan: A Guide to the IEEE 1149.4 Test
Standard A. Osseiran ISBN: 0-7923-8686-8 Design for At-
Speed Test, Diagnosis and Measurement B. Nadeau-Dosti
ISBN: 0-79-8669-8 Delay Fault Testing for VLSI Circuits A. K-
T. Cheng ISBN: 0-7923-8295-1 Research Perspectives and
Case ...

~~Essentials of Electronic Testing for Digital, Memory ...~~
Essentials of Electronic Testing for Digital, Memory, and
Mixed-Signal VLSI Circuits M. Bushnell , Vishwani Agrawal
Today's electronic design and test engineers deal with several
types of subsystems, namely, digital, memory, and mixed-

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signal, each requiring different test and design for testability methods.

~~Essentials of Electronic Testing for Digital, Memory, and ...~~

Instructor: Professor Vishwani D. Agrawal,
vagrawal@eng.auburn.edu, Broun 323, 334-844-1853. Text
book: Essentials of Electronic Testing for Digital, Memory
and Mixed-Signal VLSI Circuits by Bushnell and Agrawal,
Springer, 2000. HOMEWORK (30%): Homework 1 --
Problems 1.2 and 1.4, assigned 1/12/06, due 1/26/06,
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~~Essentials of Electronic Testing for Digital, Memory and ...~~
Copyright 2001, Agrawal & Bushnell Lecture 12: DFT and Scan 4 Scan Design Scan Design Circuit is designed using pre-specified design rules. Test structure (hardware) is added to the verified design: Add a test control (TC) primary input. Replace flip-flops by scan flip-flops (SFF) and connect to form one or more shift registers in the test mode. Make input/output of each scan shift register controllable/observable from PI/PO. Use combinational ATPG to obtain tests for all testable faults in ...

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~~EECS 579 Fall 2002 Home Page~~

Title: Testing in the Fourth Dimension Author: pagrawal Last modified by: Leon Li Created Date: 11/3/2000 2:09:08 AM Document presentation format

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The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students. Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device technology, circuit design, and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught

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before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signal subsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits. We have written this textbook for an undergraduate “ foundations ” course on electronic testing. Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course. With equal tenacity, we address the needs of three other groups of readers.

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Hardware Security: A Hands-On Learning Approach provides a broad, comprehensive and practical overview of hardware security that encompasses all levels of the electronic hardware infrastructure. It covers basic concepts like advanced attack techniques and countermeasures that are illustrated through theory, case studies and well-designed, hands-on laboratory exercises for each key concept. The book is ideal as a textbook for upper-level undergraduate students studying computer engineering, computer science, electrical engineering, and biomedical engineering, but is also a handy reference for graduate students, researchers and industry professionals. For academic courses, the book contains a robust suite of teaching ancillaries. Users will be able to access schematic, layout and design files for a printed

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circuit board for hardware hacking (i.e. the HaHa board) that can be used by instructors to fabricate boards, a suite of videos that demonstrate different hardware vulnerabilities, hardware attacks and countermeasures, and a detailed description and user manual for companion materials. Provides a thorough overview of computer hardware, including the fundamentals of computer systems and the implications of security risks Includes discussion of the liability, safety and privacy implications of hardware and software security and interaction Gives insights on a wide range of security, trust issues and emerging attacks and protection mechanisms in the electronic hardware lifecycle, from design, fabrication, test, and distribution, straight through to supply chain and deployment in the field

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This book provides the foundations for understanding hardware security and trust, which have become major concerns for national security over the past decade. Coverage includes security and trust issues in all types of electronic devices and systems such as ASICs, COTS, FPGAs, microprocessors/DSPs, and embedded systems. This serves as an invaluable reference to the state-of-the-art research that is of critical significance to the security of, and trust in, modern society ' s microelectronic-supported infrastructures.

This book documents some of the most recent advances on the physical layer of the Internet of Things (IoT), including

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sensors, circuits, and systems. The application area selected for illustrating these advances is that of autonomous, wearable systems for real-time medical diagnosis. The book is unique in that it adopts a holistic view of such systems and includes not only the sensor and processing subsystems, but also the power, communication, and security subsystems. Particular attention is paid to the integration of these IoT subsystems as well as the prototyping platforms needed for achieving such integration. Other unique features include the discussion of energy-harvesting subsystems to achieve full energy autonomy and the consideration of hardware security as a requirement for the integrity of the IoT physical layer. One unifying thread of the various designs considered in this book is that they have all been fabricated and tested in an

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advanced, low-power CMOS process, namely GLOBALFOUNDRIES 65nm CMOS LPe.

Single-threaded software applications have ceased to see significant gains in performance on a general-purpose CPU, even with further scaling in very large scale integration (VLSI) technology. This is a significant problem for electronic design automation (EDA) applications, since the design complexity of VLSI integrated circuits (ICs) is continuously growing. In this research monograph, we evaluate custom ICs, field-programmable gate arrays (FPGAs), and graphics processors as platforms for accelerating EDA algorithms, instead of the general-purpose single-threaded CPU. We study applications which are used in key time-consuming steps of

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the VLSI design flow. Further, these applications also have different degrees of inherent parallelism in them. We study both control-dominated EDA applications and control plus data parallel EDA applications. We accelerate these applications on these different hardware platforms. We also present an automated approach for accelerating certain uniprocessor applications on a graphics processor. This monograph compares custom ICs, FPGAs, and graphics processing units (GPUs) as potential platforms to accelerate EDA algorithms. It also provides details of the programming model used for interfacing with the GPUs.

Three-dimensional (3D) integration of microsystems and subsystems has become essential to the future of

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semiconductor technology development. 3D integration requires a greater understanding of several interconnected systems stacked over each other. While this vertical growth profoundly increases the system functionality, it also exponentially increases the design complexity. Design of 3D Integrated Circuits and Systems tackles all aspects of 3D integration, including 3D circuit and system design, new processes and simulation techniques, alternative communication schemes for 3D circuits and systems, application of novel materials for 3D systems, and the thermal challenges to restrict power dissipation and improve performance of 3D systems. Containing contributions from experts in industry as well as academia, this authoritative text: Illustrates different 3D integration approaches, such as

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die-to-die, die-to-wafer, and wafer-to-wafer Discusses the use of interposer technology and the role of Through-Silicon Vias (TSVs) Presents the latest improvements in three major fields of thermal management for multiprocessor systems-on-chip (MPSoCs) Explores ThruChip Interface (TCI), NAND flash memory stacking, and emerging applications Describes large-scale integration testing and state-of-the-art low-power testing solutions Complete with experimental results of chip-level 3D integration schemes tested at IBM and case studies on advanced complementary metal-oxide-semiconductor (CMOS) integration for 3D integrated circuits (ICs), Design of 3D Integrated Circuits and Systems is a practical reference that not only covers a wealth of design issues encountered in 3D integration but also demonstrates their impact on the

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efficiency of 3D systems.

This book contains extended and revised versions of the best papers presented at the 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019, held in Cusco, Peru, in October 2019. The 15 full papers included in this volume were carefully reviewed and selected from the 28 papers (out of 82 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge

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research fields like heterogeneous, neuromorphic and brain-inspired, biologically-inspired, approximate computing systems.

This book contains extended and revised versions of the best papers presented at the 26th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2018, held in Verona, Italy, in October 2018. The 13 full papers included in this volume were carefully reviewed and selected from the 27 papers (out of 106 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-

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scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge research fields like heterogeneous, neuromorphic and brain-inspired, biologically-inspired, approximate computing systems.

Emphasizes the Basic Principles of Computational Arithmetic and Computational Structure Design Taking an interdisciplinary approach to the nanoscale generation of computer devices and systems, Computer Arithmetics for Nanoelectronics develops a consensus between computational properties provided by data structures and phenomenological properties of nano and molecular technology. Covers All Stages of the Design Cycle, from Task

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Formulation to Molecular-Based Implementation The book introduces the theoretical base and properties of various data structures, along with techniques for their manipulation, optimization, and implementation. It also assigns the computational properties of logic design data structures to 3D structures, furnishes information-theoretical measures and design aspects, and discusses the testability problem. The last chapter presents a nanoscale prospect for natural computing based on assorted computing paradigms from nature. Balanced Coverage of State-of-the-Art Concepts, Techniques, and Practices Up-to-date, comprehensive, and pragmatic in its approach, this text provides a unified overview of the relationship between the fundamentals of digital system design, computer architectures, and micro-

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and nanoelectronics.

Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies

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and EDA solutions for testing low power devices.

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